NTMX82CA

Product description

The NTMX82AA Dual PCM30 interface card provides a link between CPM shelves and co–located transmission equipment. Office repeaters and channel banks are co–located transmission equipment.

This dual PCM30 interface uses a new pack size (packlet) that is 1/6th of the standard DMS–100 size. The packlet is the same as the dual DS1 interface NTMX81.

The NTMX82CA is an improved version of the NTMX82CA card which incorporates minor hardware changes in order to support the Loss Of Signal (LOS) alarm indication.

Location

Four packlets fit in a quad frame carrier. The quad carrier frame occupies a standard size CPM slot. The quad frame carrier is NTMX87.

Functional description

The NTMX82CA Dual PCM30 interface contains:

- application–specific integrated circuit (ASIC)
- Conference of European Postal and Telecommunications (CEPT) Administrations transceiver DS2181A
- line interface integrated circuit and power feed switching

Application–specific integrated circuit (ASIC) functional blocks

The NTMX82CA has the following ASIC functional blocks:

- bidirectional serial interface between a DS60 line and two DS2181A PCM30 transceivers
- select the active DS60 line from own or mate DS60 according to an activity pin
- generate the 5.12 MHz and 2.56 MHz internal clocks and the 2.048 MHz system clock from the 10.24 MHz clock input
- generate synchronization pulses for the PCM30 transceiver and for the internal elastic buffer
- loopback for each timeslot—The ASIC extracts a timeslot from the outgoing PCM30 stream to the DS2181A transceiver. The ASIC inserts a timeslot in the incoming PCM30 stream. Each timeslot, except for timeslot 0, can loop back according to a software controlled register.

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- Message control channel—The ASIC provides a bidirectional interface for the DMSX message between the message pack and the host switch. The ASIC inserts the message received from the message pack on timeslot 1 or 16 of the outgoing PCM30 stream. In the opposite direction, the ASIC extracts the message received on timeslot 1 or 16. The ASIC sends the message to the message pack. The software selects timeslot 1 or 16 for the message channel.
- signaling buffer—The ASIC stores and inserts timeslot 16 of the incoming PCM30 stream. The ASIC inserts the timeslot as timeslot 16 in a specified frame of the 16–frame multiframe. The incoming PCM30 stream contains the signaling information. The signaling buffer operates when the Channel Associated Signaling mode is active.
- slip counter—The ASIC samples slip output of the internal elastic buffer. An 8–bit counter registers the number of slips.
- timeslot 0 odd—The ASIC detects an odd timeslot 0 out of the 16–frame multiframe. The ASIC sends the timeslot to the matrix pack. In the opposite direction, the ASIC controls the odd timeslot 0 the DS2181A transceiver sends.
- serial interface—A serial bidirectional interface controls each DS2181A transceiver. The ASIC accesses each register of the DS2181A in read/write or read–only mode.
- CRC4 error indication bits (E–bits)—These E–bits indicate sub–multiframes that contains errors. On the transmit side, the ASIC inserts two E–bits in the outgoing data stream. The hardware circuit or the software–loop register provide these bits. On the receive side, the ASIC extracts two E–bits from the incoming data stream. The ASIC inserts the E–bits in the odd register.
- E–bit count register (EBCR)—The EBCR register counts the E–bits received in the incoming data.
- facility data link (FDL)—This function creates a communication link. On the transmit side, the ASIC inserts FDL bits in the odd frames of the outgoing data. The FDL register provides the FDL bits. On the receive side, the ASIC inserts FDL bits in the FDL register. The odd frames of the incoming data provide the FDC bits.
- international bits (INB)—On the transmit side, the ASIC inserts INB in the odd and even frames of the outgoing data. The loop register provides the INB. On the receive side, the ASIC inserts the INB in the odd register. The odd and even frames of the incoming data provide the INB.

- blanking data interface—The ASIC inserts all ones in the channels (1–31) sent to the matrix, after loss of frame synchronization (RFSA=1).
- internal elastic store—There is an elastic store of two frames depth. The store slips on the frame boundary. The store has slip detection and control.

Conference of European Postal and Telecommunications (CEPT) administrations transceiver DS2181A functional blocks

The NTMX82CA has the following CEPT transceiver DS2181A functional blocks:

- primary rate transceiver to execute International Telegraph and Telephone Consultative Committee (CCITT) standards
- supports cyclic redundancy check–4 (CRC4)–based framing standards
- supports common associated signaling (CAS) and common channel signaling (CCS) signaling standards
- contains on–chip alarm generation, alarm detection, and error logging logic
- operates with the DS2175 elastic store or with the internal elastic store in the ASIC

Line interface integrated circuit functional blocks

The NTMX82CA has the following line interface integrated circuit functional blocks:

- wave shaping according to CCITT
- clock recovery
- CEPT input amplifier (with AGC)
- physical line driving and receiving
- input jitter attenuator

Power feed switching functional blocks

The NTMX82CA has the following power feed switching functional blocks:

- power supply redundancy—the feed circuits change the power source from the own power supply to the mate power supply. This event occurs when the own power supply fails
- blown fuse indication—a special detection logic that detects and sets a bit if a fuse blows. The redundant fuses on the pack provides this feature.

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Signaling

Pin numbers

The pin numbers for the NTMX82CA appear in the following table.

NTMX82CA pin numbers

Pin	A	B	C	D
1	GND	T1IN/C1	T1INM/C1	–
2	C97	T1INM/P0	T1OUT/P0	–
3	–ACT	T1INM/P1	T1OUT/P0	–
4	C324	T1INM/C0	T1OUT/C0	–
5	SENDT0	+5VM	T1OUT/C1	–
6	SENDR0	FRPC1	T1OUTM/P0	–
7	SENDT1	–FP48M	T1OUTM/P1	–
8	SENDR1	C324M	T1OUTM/C0	–
9	RECT0	P/–C	T1OUTM/C1	–
10	RECR0	–U0/U1	MSGIN0	–
11	RECT1	+12V	MSGOUT	–
12	RECR1	–12V	FPRC0	–
13	C97M	+12VM	FPRC0M	–
14	T1IN/P0	–12VM	FP48–	–
15	T1IN/91	T1IN/C0	–	–
16	GND	MSGEN	+5V	–

Note: Blank cells indicate pins that are not in use.

Technical data

The dual PCM30 packlet consumes the following:

Power requirements

The power requirements for the NTMX82CA appear in the following table.

Power requirements

Voltage	Current
+5 V	300 mA
+12 V	3 mA
–48 V	——

Environmental requirements

The environmental requirements for the NTMX82CA follows:

1. Ambient air temperature: <70 deg C
2. Relative humidity: 20–80% for short term; 20–55% normal